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UNITED STATES PATENT APPLICATION

FOR

WAFER REUSE TECHNIQUES

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WAFER REUSE TECHNIQUES

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Field

[0001] The subject matter disclosed herein generally relates to silicon wafer reuse techniques.

Description of Related Art

[0002] Test and monitor silicon wafers are typically used in larger numbers in both new process development and manufacturing testing procedures. For example, FIG. 1 depicts a prior art process in which a single crystal silicon wafer is used to test new process development and manufacturing testing procedures in semiconductor tools. After testing the tool, the wafer is chemically etched to remove any surface contaminants. Next, the wafer can be surface polished. Thereafter, the wafer may be reused to qualify the same or a different semiconductor tool. Polishing the wafer results in the progressive thinning of the wafer, due to material removal, thus limiting the number of times the wafer can be reused. Currently test wafers are reused only once. Further, because of possible metal contamination concerns, reused wafers are typically limited to use for limited purposes (e.g., back end processes) and so have a limited range of capabilities to test new process development and test procedures in semiconductor tools. These test and monitor wafers represent a large cost item and do not generate revenue. It is desirable to test semiconductor tools in as low a cost manner as possible.

Brief Description of the Drawings

[0003] FIG. 1 depicts a prior art process in which a single crystal silicon wafer is used to test a semiconductor tool; and

[0004] FIG. 2 depicts a flow diagram of a process in accordance with one embodiment of the present invention; and

[0005] FIG. 3 depicts wafers that can be used in the process of FIG. 2.

[0006] Note that use of the same reference numbers in different figures indicates the same or like elements.

Detailed Description

[0007] FIG. 2 depicts a flow diagram of a process in accordance with one embodiment of the present invention that provides at least for multiple and potentially unlimited reuse of test wafers. FIG. 3 depicts wafers that can be used in the process of FIG. 2. In action 210, a silicon wafer (such as a single crystal silicon wafer or a low cost polycrystalline wafer) may be provided. The silicon wafer of action 210 may correspond to wafer 300 of FIG. 3. For example, low cost polycrystalline wafers can be made from cast ingots. For example, one suitable technique to fabricate low cost polycrystalline wafers is described in U.S. Patent No. 6,406,981, although other techniques and/or wafers may be used.

[0008] In action 220, the silicon wafer may be coated with polysilicon. For example, action 220 may include using a chemical vapor deposition (CVD) process to coat at least the flat top and flat bottom surfaces of the wafer with polysilicon. A suitable thickness of the polysilicon may be approximately five (5) microns or less, although other thicknesses may be

used. For example, to provide polysilicon, a suitable CVD process may include (1) using a vertical diffusion furnace to heat multiple stacked silicon wafers; (2) adding $SiCl_3$, SiH_4, or $SiHCl_3$; and (3) heating the stacked wafers to about 600°C for approximately 2 to 4 hours. The polysilicon coated wafer of action 220 may correspond to coated wafer 310 of FIG. 3.

[0009] In action 230, the flat surfaces of the wafer coated with polysilicon may be polished. Action 230 may include utilizing chemical mechanical polishing (CMP). The surface polished polysilicon coated wafer of action 230 may correspond to polished coated wafer 315 of FIG. 3. For example, the polished surfaces may behave as a single crystal structure when analyzed using metrology tools. In one embodiment, the grain size of the polished surface of the polysilicon layer may be submicron size. In one embodiment, the polished surface of the polysilicon layer may create an insignificant distortion of the angle of refraction of incident light. The polished surface may also have very low density of light scattering defects as detected by a surface scan tool.

[0010] In one implementation, depositing and polishing the polysilicon layer results in very low contaminant (e.g., metal) levels at the wafer surface, similar to current single crystal based test wafers. Consequently, reused wafers may be used as virgin test wafer with no limitation as to semiconductor tools in which the wafer can be used, unlike the case for current test wafers.

[0011] In action 240, the surface polished coated wafer is used to test a semiconductor tool. For example, wafers with low light scattering properties can be used to test and qualify semiconductor wafer processing tools for their propensity to add particles to the wafer, where such added particles may scatter light. For example, to test film application by a semiconductor tool, film may be provided over the polished coated wafer and the thickness, uniformity of

thickness of the film, and particles (light scattering defects) added by the process tool may be determined.

[0012] In action 245, surface contaminants (such as films and materials) formed on the polysilicon coating of the wafer after use in the semiconductor tool may be removed. For example, action 245 may include removing surface metals (such as copper, nitride, oxide, titanium nitride, or any film) provided over the surface of the test wafer after testing in action 240. For example, action 245 may include using chemical etching techniques such as SC1-SC2 clean.

[0013] In action 250, the coating may be removed from the test wafer used to test a semiconductor tool. For example, action 250 may include using mechanical grinding techniques to remove the polysilicon coating from the test wafer. The test wafer removed of films and materials formed on the polysilicon coating and its polysilicon coating may correspond to stripped wafer 320 of FIG. 3.

[0014] In action 260, a new coating may be provided over the wafer 320. For example, techniques similar to those described with respect to action 220 may be utilized. The wafer provided with the new coating may correspond to refreshed coated wafer 330 of FIG. 3. Action 230 may follow action 260. In the next execution of action 230, the wafer with the new polysilicon coating may be polished. In one implementation, wafer reuse primarily involves dry steps with the exception of chemical wafer cleaning. This substantially minimizes the potential for metal contamination on the surface of polished wafers.

Modifications

[0015] The drawings and the forgoing description gave examples of the present invention. The scope of the present invention, however, is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of the invention is at least as broad as given by the following claims.